AMENDMENTS TO THE CLAIMS:

Please cancel without prejudice claims 1-8 and 16-23 and amend claims 9 and 24 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (cancelled).

2. (cancelled).

3. (cancelled).

4. (cancelled).

5. (cancelled).

6. (cancelled).

7. (cancelled).

8. (cancelled).

9. (currently amended) Apparatus for processing data, said apparatus comprising:

a cache memory operable to store program instructions to be executed; ~~and~~

an instruction pipeline including an instruction prefetch unit; and

an exception controller, responsive to an exception signal signaling an exception, ~~to~~ ~~trigger~~for triggering exception processing by forcing program execution starting from an exception handling program instruction stored at a predetermined memory location; wherein upon receipt of said exception signal part way through execution of a current program instruction, said exception controller ~~is operable to trigger~~triggering a lookup of said exception

handling program instruction within said cache memory and, if said exception handling program instruction is not present within said cache memory, ~~to trigger~~triggering a cache linefill operation to read said exception handing program instruction from a main memory to said cache memory, and, upon completion of execution of said current program instruction, if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory.

10. (original) Apparatus as claimed in claim 9, wherein execution of said current instruction lasts for a plurality of clock cycles and lookup of said exception handling program instruction within said cache memory starts part way through said plurality of clock cycles.

11. (original) Apparatus as claimed in claim 9, wherein said exception handling program instruction redirects program execution to an exception handling routine.

12. (original) Apparatus as claimed in claim 9, wherein said exception controller is an interrupt controller, said exception signal is an interrupt signal and said exception handling program instruction is and interrupt handling program instruction.

13. (original) Apparatus as claimed in claim 9, wherein said exception is one of a data abort and a prefetch abort.

14. (original) Apparatus as claimed in claim 9, wherein said cache memory and said exception controller are parts of a processor core.

15. (original) Apparatus as claimed in claim 9, wherein said apparatus is an integrated circuit.

16. (cancelled).

17. (cancelled).

18. (cancelled).

19. (cancelled).

20. (cancelled).

21. (cancelled).

22. (cancelled).

23. (cancelled).

24. (currently amended) A method of processing data, said method comprising the steps of:

storing program instructions to be executed within a cache memory; ~~and~~

processing program instructions with an instruction pipeline including an instruction prefetch unit; and

triggering, in response to an exception signal, ~~triggering~~ exception processing by forcing program execution starting from an exception handling program instruction stored at a predetermined memory location; wherein, upon receipt of said exception signal part way through execution of a current program instruction, said triggering step includes triggering a lookup of said exception handling program instruction within said cache memory and, if said exception

handling program instruction is not present within said cache memory, said triggering step includes triggering ~~to trigger~~ a cache linefill operation to read said exception handing program instruction from a main memory to said cache memory, and, upon completion of execution of said current program instruction, if said exception is still current, then said instruction prefetch unit fetches said exception handling program instruction from said cache memory.

25. (original) A method as claimed in claim 24, wherein execution of said current instruction lasts for a plurality of clock cycles and lookup of said exception handling program instruction within said cache memory starts part way through said plurality of clock cycles.

26. (original) A method as claimed in claim 24, wherein said exception handling program instruction redirects program execution to an exception handling routine.

27. (original) A method as claimed in claim 24, wherein said exception signal is an interrupt signal and said exception handling program instruction is and interrupt handling program instruction.

28. (original) A method as claimed in claim 24, wherein said exception is one of a data abort and a prefetch abort.

29. (original) A method as claimed in claim 24, wherein said method is performed within a processor core.

30. (original) A method as claimed in claim 24, wherein method is performed within an integrated circuit.